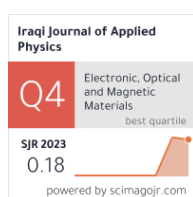


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Effect of Silver Content and Post-Deposition Annealing on Electrical Properties of CAZTSe Thin Films and Their Heterojunction Diodes

In this study, the effect of Ag content and annealing temperature on the electrical properties of polycrystalline $(\text{Cu}_{1-x}\text{Ag}_x)_2\text{ZnSnSe}_4$ thin films and the C-V characteristics of Al/n-CdS/p-CAZTSe/n-Si/Al heterojunction diodes are investigated. The Ag content (x) and the annealing temperature (T_a) were chosen to be (0.0, 0.1, and 0.2) and (373 and 473) K, respectively. The results showed that all the prepared thin films exhibit p-type conductivity and that the hole concentration decreases with increasing x and T_a . Additionally, the width of the depletion region and the potential barrier of all the manufactured diodes, which are of the abrupt type, increase with the increase of x and T_a .

Keywords: CAZTSe; Thin films; Heterojunction diodes; Polycrystalline

Received: 21 June 2024; Revised: 18 August 2024; Accepted: 25 August 2024

1. Introduction

The indium-free quaternary chalcogenide, $\text{Cu}_2\text{ZnSnSe}_4$ (CZTSe), is of significant interest for potential applications in optoelectronics and photovoltaics [1,2] due to its advantageous properties such as a suitable direct energy gap, high absorption coefficient, non-toxicity, and the abundance of its constituent elements. The electrical characteristics of CZTSe can be modified through alterations in stoichiometry and/or appropriate doping [3-6]. CZTSe possesses various inherent defects, including interstitials, vacancies, and antisite defects, which are classified as either electron acceptors or electron donors [7] depending on the valence of the elements involved. Due to their low formation energy, Cu_{Zn} antisite defects, which act as acceptor defects, are predominant in CZTSe [8]. This predominance is attributed to the similar ionic radii of Cu and Zn, which are 0.91Å and 0.88Å, respectively, resulting in CZTSe typically exhibiting p-type conductivity [9]. To enhance the physical properties of the quaternary compound $\text{Cu}_2\text{ZnSnSe}_4$, it is crucial to reduce the density of Cu_{Zn} acceptor defects. Ag is a promising candidate to replace Cu due to its atomic radius being about 16% larger than that of Cu and its membership in the same chemical group as Cu [10,11]. The substitution of Cu with Ag on the Cu-sublattice decreases the Cu_{Zn} defect density since the formation energy of Ag_{Zn} defects (3.1 eV) is higher than that of Cu_{Zn} defects (1.41 eV) [12]. $\text{Cu}_2\text{ZnSnSe}_4$ thin films can be prepared using both vacuum and non-vacuum techniques. In the vacuum technique, various

deposition parameters can be controlled to achieve the desired crystalline quality and stoichiometric ratio [13,14].

2. Experimental Procedure

To investigate the electrical properties of thin CAZTSe films deposited on corning glass substrates and Al/CdS/CAZTSe/Si/Al HJDs, several steps were followed. $(\text{Cu}_{1-x}\text{Ag}_x)_2\text{ZnSnSe}_4$ alloys with varying Ag content ($x = 0.0, 0.1$, and 0.2) were prepared as detailed in our previous paper [15]. The glass substrates were cleaned both chemically and ultrasonically using a cleaning solution, distilled water, ultrasonic detergent, and alcohol with 99.999% purity. The single crystal Si wafer substrates with (111) orientation were carefully cleaned by immersing and stirring them in a diluted hydrofluoric acid (HF) solution (1:10 with distilled water) for 10 minutes to remove the oxide layer formed due to environmental exposure. Next, the substrates were rinsed with distilled water for a few minutes and then dried with hot air. To perform electrical measurements of CAZTSe thin films and their fabricated heterojunction diodes, 200 nm thick aluminum electrodes were deposited using a thermal evaporation technique with a spiral tungsten boat. Prior to deposition, masks made from thick aluminum foil were placed on the glass substrates to define the electrode shapes. Additionally, a thin layer of aluminum was deposited on the anti-reflective side of the Si substrates. An appropriate amount of prepared CAZTSe alloy powder, depending on the value of x, achieving the required

thickness of 800 nm was placed in a molybdenum boat equipped with a cover with suitable holes to prevent diffusion of the material during the evaporation process. The boat was installed between two electrodes in the vacuum chamber and at a distance of 18 cm from the metal substrate holder. When the pressure inside the vacuum system reached 10^{-5} torr, an electric current was passed through the boat gradually, and when the temperature of the boat reached the point of powder evaporation, the deposition process began at a rate of 0.53 nm/s on both types of substrates, (Al-electrodes/glass) and (n-Si/Al-thin layer), and after the entire material evaporated, the current was gradually reduced to zero. After this process we obtained CAZTSe/electrodes/glass and CAZTSe/n-Si/Al structures, respectively. The same steps were used to grow thin CdS films on CAZTSe/Si/Al structures with thickness of 100 nm and deposition rate of 0.3 nm/s using ready-made CdSe alloy powder which provided from Balzers Company with high purity of 99.999%. The prepared samples were left under high vacuum for one day. Some samples were annealed at 373 and 473 K under vacuum for one hour. Finally, Al front electrodes were deposited on CdS/CAZTSe/Si/Al structures using appropriate masks. This represents the final step to complete the fabrication of CAZTSe HJDs.

The electrical properties of thin CAZTSe films were studied using d.c. conductivity and Hall Effect measurements. For d.c. measurements, electrical resistance was measured as a function of temperature for different values of x and Ta, within temperature range 318-488 K, using a Keithley 616 model. The resistivity of these films was obtained using the following equation [16]:

$$\rho = \frac{RA}{L} \quad (1)$$

where R and A are the film resistance and cross-sectional area, respectively and L is the distance between the electrodes. Additionally, the conductivity can be expressed as [17]:

$$\sigma_{d.c} = \frac{1}{\rho} \quad (2)$$

The activation energies (E_{a1} and E_{a2}) were calculated using Arrhenius equation [18]:

$$\sigma_{d.c} = \sigma_o \exp\left(-\frac{E_a}{k_B T}\right) \quad (3)$$

where σ_o is a constant, k_B is a Boltzmann's constant and T is an absolute temperature. Hall Effect measurements were conducted using two Keithley models 616 to measure Hall voltage (V_H) as a function of current (I) at a constant magnetic field (B)

Hall coefficient (R_H), holes concentration (P), and Hall mobility (μ_H) were determined using the relationships below, respectively [17]:

$$R_H = \left(\frac{V_H}{I}\right)\left(\frac{t}{B}\right) \quad (4)$$

where t is the thickness of thin films

$$P = \frac{1}{qR_H} \quad (5)$$

where q is an electron charge

$$\mu_H = \frac{|R_H|}{\rho} = |R_H|\sigma \quad (6)$$

For capacitance-voltage (C-V) measurements, the capacitance of all Al/CdS/CAZTSe/Si/Al heterojunction diodes was examined in the dark at fixed frequency of 100 kHz as a function of reverse bias voltage in the range of 0.1-2 V using LCR meter of type Gwinstek 8105G.

The capacitance per unit area and the width of the depletion region of the HJDs were estimated using the following equations [17,19]:

$$C_j = \frac{C}{A_j} = \left[\frac{q\epsilon_n\epsilon_p N_d N_a}{2(\epsilon_n N_d + \epsilon_p N_a)} \right]^{\frac{1}{2}} (V_{bi} - V)^{-\frac{1}{2}} \quad (7)$$

where ϵ_n and ϵ_p are the permittivity of n and p-type semiconductors, respectively, N_a and N_d are the acceptor and donor concentrations, respectively, V_{bi} is the junction built-in potential, and V is the applied voltage in reverse bias

$$W = \frac{\epsilon_s}{C_0} \quad (8)$$

where C_0 is the capacitance of diode at zero bias voltage, and ϵ_s is the semiconductor permittivity for the two semiconductor materials, given by the following equation:

$$\epsilon_s = \frac{\epsilon_n \epsilon_p}{\epsilon_n + \epsilon_p} \quad (9)$$

3. Results and Discussion

Figure (1a-c) shows the variation of d.c. electrical conductivity ($\sigma_{d.c}$) with temperature (T) in the form of $\ln\sigma$ as a function of $1000/T$ plots for as deposited and annealed thin $(\text{Cu}_{1-x}\text{Ag}_x)_2\text{ZnSnSe}_4$ films with different Ag content. It can be seen from this Figure that the d.c. conductivity of all examined samples increases with increasing the temperature in the range RT-488K, this means that all samples have a negative thermal coefficient with resistivity and this is an essential property of semiconductor [20-22]. The plot of $\ln\sigma_{d.c}$ versus $1000/T$ are not completely linear and showing two clear different regions and the activation energies E_{a1} , E_{a2} are calculated from the slopes of the curves in both regions using formula (3). The presence of two activation energies in thin CAZTSe films confirms the polycrystalline nature for these films. The first activation energy (E_{a1}) occurs at relatively higher temperature within the range 348-488K. The conduction mechanism of E_{a1} is due to carriers excited beyond the mobility edges into extended states, while the second activation energy (E_{a2}) occurs at relatively lower temperature within the range 318-348K, and the conduction mechanism of this stage is due to carriers transport to the localized states near the valence and conduction band edge [23]. Table (1) displays the values of the two activation energies and the electrical conductivity of thin CAZTSe films with different Ag content and annealing temperature. It is evident that the values of E_{a1} and E_{a2} are decreased with increasing x and T_a . The decreasing in the activation energy with increasing x and T_a is expected because the energy

gap decreases with increasing x value and T_a as reported in our previous paper [4] which in turn led to an increase in the electrical conductivity of the thin films with increasing x content and T_a .

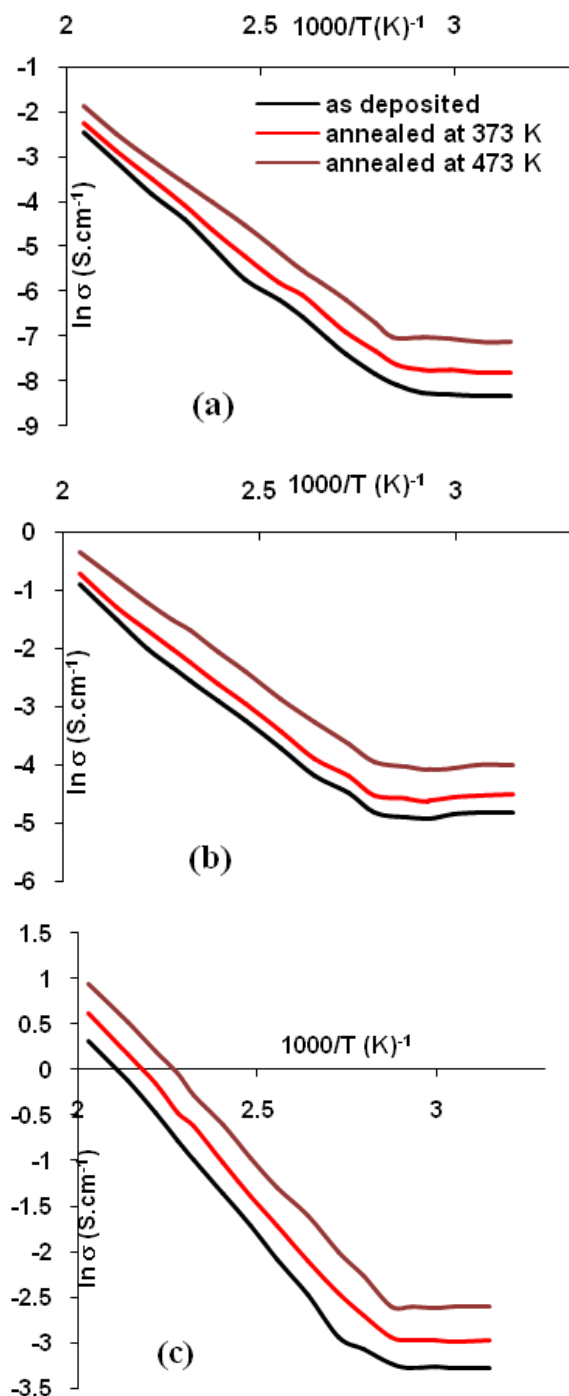


Fig. (1) $\ln \sigma$ vs. $(1000/T)$ for as deposited and annealed CAZTSe thin films at (a) $x=0.0$, (b) $x=0.1$ and (c) $x=0.2$

As complementary work, the Hall measurements have been used to determine the charge carrier type, concentration and Hall mobility for as deposited and annealed CAZTSe thin films with different Ag content using Eqs. (4), (5) and (6), respectively and the results are listed in table (2). As seen from table (2), the sign of Hall coefficient (R_H) is positive

which means that all the samples exhibit p-type conductivity, i.e., holes are predominant in the conduction process. This result agrees with the previous studies [24-28] where they confirmed that the pure Cu thin films show p-type conductivity. While, Henry *et. al.* [26] confirmed that the conductivity of CAZTSe films remains of p-type even after adding Ag with content less than 50%. The natural p-type behavior of CZTSe is attributed to its acceptor intrinsic point defects especially Cu_{Zn} acceptor antisite defects which are produced in high concentration due to the similarity of Cu and Zn ionic radius, which results in low formation energy [29-31].

Table (2) Electrical parameters from Hall effect measurements for CAZTSe thin films with different Ag content and annealing temperature

x	T_a (K)	R_H (cm^3/C)	$P_H \cdot 10^{17}$ (cm^{-3})	μ_H ($\text{cm}^2/\text{V.s}$)
0.0	R.T	7.0263	8.8951	0.0792
	373	7.2812	8.5837	0.1068
	473	7.5891	8.2354	0.1708
0.1	R.T	9.0242	6.9258	0.6354
	373	9.2893	6.7281	0.8397
	473	9.7607	6.4032	1.4022
0.2	R.T	12.1602	5.1397	3.5175
	373	12.5549	4.9781	5.0032
	473	13.0684	4.7825	7.5091

From table (2), it can be noticed that the concentration of the charge carriers decreases with increasing Ag content and annealing temperature. The reduction in holes concentration with increasing Ag content can be explained based on the corresponding reduction in the acceptor point defects density (V_{Cu} and Cu_{Zn}) [32,33]. With increasing Ag content, there is less Cu and more Ag on the Cu-sublattice and this in turn causes a decrease in the density of antisite defects Cu_{Zn} and V_{Cu} . At the same time, the formation energies for point defect V_{Ag} and Ag_{Zn} which are 2.14 and 3.1 eV, respectively [34] are high compared to the formation energies for the V_{Cu} and Cu_{Zn} which are 1.14 and 1.41 eV, respectively [35]. So, Ag occupied Cu-sublattice sites are less likely to contribute for Ag_{Zn} and V_{Ag} . A similar result was obtained by G. Talia *et. al.* and Douglas *et. al.* [36,37]. Another observation is that the holes mobility increases with increasing Ag content and annealing temperature, and this can be attributed to the decrease in the holes concentration which in turn causes a decrease in the number of collisions between them and consequently an increase in their mobility (Hall mobility is inversely proportional to the concentration of the carriers).

Figure (2a-c) presents the relation between inverse capacitance squared for all the prepared heterojunction as function of the reverse bias voltage. The linearity of $1/C^2$ -V characteristics indicates that the junction is an abrupt [38,39]. From the intercept of the straight line with x-axis and y-

axis, the values of V_{bi} and C_o were obtained, respectively while the carrier concentration was deduced from the slope of the straight line using Eq. (7). Finally, the depletion region width was calculated using Eq. (8).

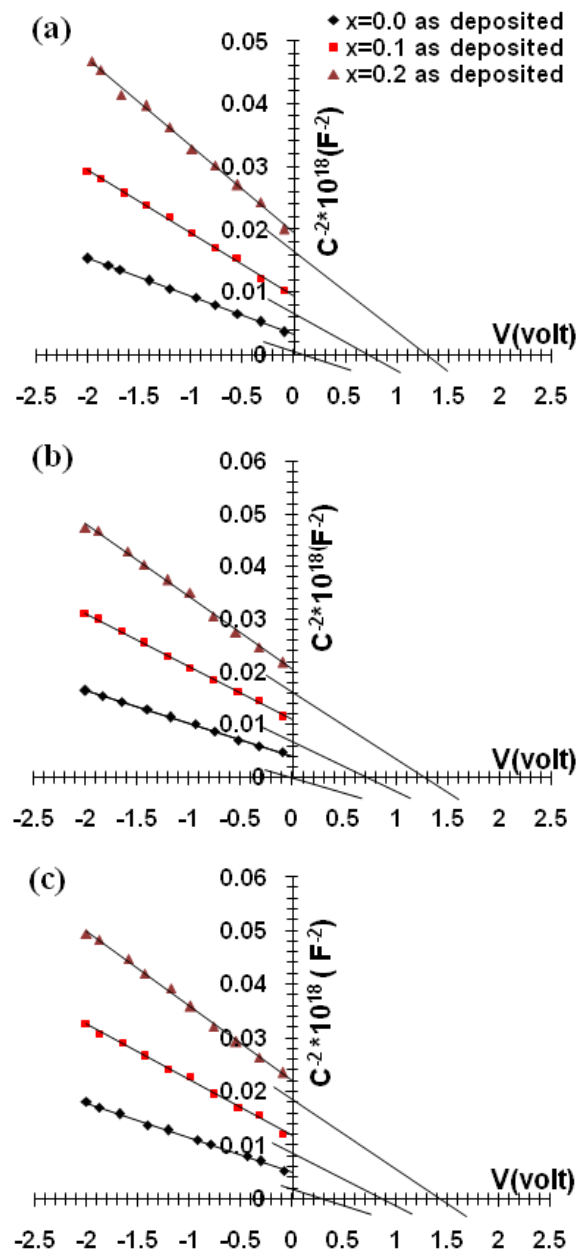


Fig. (2) Variation of C^{-2} as a function of applied voltage (V) for (a) as-deposited, (b) $T_a=373K$ and (c) $T_a=473K$ Al/CdS/($Cu_{1-x}Ag_x$)₂ZnSnSe₄/Si/Al heterojunction

The obtained results are listed in table (3). It is clear that the increases in both Ag content and annealing temperature led to a decrease in the carrier concentration, which in turn decrease the zero bias capacitance and increase the value of the built-in potential and the depletion region width. The calculated carrier concentration is smaller than that obtained from Hall Effect measurement. This difference is attributed to the different measurement

method [40], or it may be attributed to the occurrence of the diffusion process, which confirms the formation of the junction. A thicker depletion region is preferred to separate photo generated e-h pairs but causes high resistivity [40,41].

Table (3) C-V measurement Parameters for as deposited and annealed Al/CdS/($Cu_{1-x}Ag_x$)₂ZnSnSe₄/Si/Al heterojunction

T_a (K)	V_{bi} (volt)	$C_o \times 10^{-9}$ (F/cm ²)	W (μ m)	$N_p \times 10^{16}$ (cm ⁻³)
R.T	0.52	29.934217	0.147660	1.228947
373	0.6	26.688025	0.165620	1.194799
473	0.7	24.056261	0.183739	1.135306
R.T	0.95	17.190354	0.263355	0.579702
373	1.05	16.112274	0.281595	0.564877
473	1.1	15.474611	0.293199	0.550411
R.T	1.4	11.996929	0.387716	0.365429
373	1.5	11.697706	0.397633	0.362256
473	1.57	11.288091	0.412062	0.359188

4. Conclusions

The electrical properties of pure copper zinc tin selenide (CZTSe) thin films improved after adding silver (Ag) with contents of 0.1 and 0.2 and annealing at temperatures of 373 K and 473 K. Al/n-CdS/P-CAZTSe/n-Si/Al heterojunction diodes (HJDs) were successfully fabricated using the vacuum thermal evaporation technique. The capacitance and carrier concentration values of the fabricated diodes decreased, while their depletion region width and built-in potential values increased with increasing Ag content and annealing temperature. These results suggest that CAZTSe-based diodes are a good candidate for the fabrication of high-performance heterojunction solar cell diodes.

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Table (1) Electrical parameters from D.C conductivity measurement for CAZTSe thin films with different Ag content and annealing temperature

x	T _a (K)	$\sigma_{R,T} \times 10^{-2}$ (S.cm ⁻¹)	E _{a1} (eV)	Temp. Range (K)	E _{a2} (eV)	Temp. Range (K)
0.0	R.T	1.1276	0.6212	348-488	0.0568	318-348
	373	1.4671	0.5858	348-488	0.0458	318-348
	473	2.2511	0.5486	348-488	0.0374	318-348
0.1	R.T	7.0416	0.4426	348-488	0.0347	318-348
	373	9.0399	0.4340	348-488	0.0299	318-348
	473	14.3658	0.4139	348-488	0.0171	318-348
0.2	R.T	28.9266	0.3948	348-488	0.0135	318-348
	373	39.8509	0.3819	348-488	0.0092	318-348
	473	57.4599	0.3655	348-488	0.00018	318-348